Architecture 2:

Using a single N+1 FIFO to feed the FIR filter

The restriction for operation of an FIR filter is that y[n] must be computed in the following way:

I use to denote that the output y[n] is the convolution between input signals present in different channels so between two adjacent values of y[n], they are computed from two adjacent channels of input signals x.

The basic operation is that each filter tap is multiplying a datapoint of located at , with coefficient . The entire signal must be available to be fed through the FIR filter so that the correct response is generated. On each clock cycle, a separate channel needs to be used so the N+1 length FIFO will be emptied and filled with values from where N is the order of the filter.

A naïve approach illustration with 3 channels is this:

Or more generally